

TABLE I. DEVICE PARAMETERS 1/, 2/

JPL PART NO. ST12196-	JPL USAGE	MFR	MFR PART NO	PACKAGE STYLE	RADIATION LEVEL (TID) (RADS)	ELECTRICAL PERFORMANCE CHARACTERISTICS	TERMINAL CONNECTIONS	ELECTRICAL TEST REQUIREMENTS	BURN-IN CIRCUITS	OTHER REQMENTS /DETAILS
U7872UX10	FLIGHT	ADI	AD7872B	DIE 3/	TBD	TABLE III HEREIN	DIE 3/	N/A	N/A	5/
U7872FR10	FLIGHT	SEI	7872RPF-10	16-LEAD RADPAK FLATPACK 6/	TBD	TABLE III HEREIN	FIGURE 1 HEREIN	TABLE II HEREIN	TBD	7/
U7872FEM	EM	SEI	7872F-E10	16-LEAD STD FLATPACK 6/	N/A	TABLE III HEREIN	FIGURE 1 HEREIN	8C/	N/A	8/
U7872REM	EM	SEI	7872RPF-E10	16-LEAD RADPAK FLATPACK 6/	N/A	TABLE III HEREIN	FIGURE 1 HEREIN	8C/	N/A	8/
U7872REM	EM	SEI	7872RPF-E10	16-LEAD RADPAK FLATPACK 6/	N/A	TABLE III HEREIN	FIGURE 1 HEREIN	8C/	N/A	8/
U7872FXB	FLIGHT	SEI	7872FB-10	16-LEAD STD FLATPACK	N/A	TABLE III HEREIN	FIGURE 1 HEREIN	TABLE II HEREIN	FIGURES 2,3,4 HEREIN	7/

NOTES:

- 1/ THIS DRAWING IN CONJUNCTION WITH CS515577 IMPOSES ALL REQUIREMENTS FOR PROCUREMENT OF THESE DEVICES.
2/ THIS IS A SINGLE CHIP LOW POWER 14-BIT ANALOG-TO-DIGITAL CONVERTER WITH A 10µSEC CONVERSION TIME, ±1 LSB LINEARITY AND -40°C TO +85°C OPERATING TEMPERATURE RANGE.

APPLICABLE TO DICE:

- 3/ DIE PHYSICAL DIMENSIONS AND DESIGN DATA (INCLUDING THE TOP AND BACKSIDE METALLIZATIONS AND THICKNESSES) SHALL BE PROVIDED BY THE DIE MANUFACTURER. ADDITIONALLY, THE MANUFACTURER SHALL MAKE RECOMMENDATIONS ON THE DIE-ATTACH AND BONDING OPERATIONS.
4/ THE DICE SHALL BE ELECTRICALLY GOOD (MEET ELECTRICAL LIMITS OF TABLE III HEREIN) OVER -40°C TO 85°C TEMPERATURE RANGE.
5/ THE FOLLOWING ADDITIONAL REQUIREMENTS SHALL APPLY:
A. JPL WILL PERFORM VISUAL AND SEM INSPECTION PER MIL-STD-883, METHODS 2010 COND. A AND 2018 (RESPECTIVELY).
B. DICE SHALL BE STORED IN A CLEAN, DRY ENVIRONMENT AND EXTREME CARE SHALL BE TAKEN IN HANDLING THEM.
C. TRACEABILITY SHALL BE MAINTAINED FROM THE DIE TO THE INDIVIDUAL WAFER.

APPLICABLE TO PACKAGED PARTS:

- 6/ THE MANUFACTURER SHALL PROVIDE DETAILED INFORMATION ON THE PACKAGE CONSTRUCTION AND THE CASE OUTLINE (REFER TO MIL-STD-1835 FOR SPECIFYING THE CASE OUTLINE DIMENSIONS).

RELEASED THRU SECTION 356 DATA MANAGEMENT:			DATE:	
REVISION: B			APPROVED BY (Section 514):	
APPROVED SOURCE(S)			DATE:	
VENDOR PART NO.	VENDOR		JPL PART NO.	The item listed in the approved source block and identified by vendor name, address, and part number will be evaluated and tested by the JPL Electronic Parts Reliability Section or its delegated alternate before being approved for use. Non-JPL users shall check with the Electronic Parts Reliability Section on the status of the part's approval before using.
SEE TABLE I	ANALOG DEVICES, INC ONE TECHNOLOGY WAY NORWOOD, MA 02062 CAGE CODE 24355		SPACE ELECTRONICS, INC 4031 SORRENTO VALLEY BLVD SAN DIEGO, CA 92121 CAGE CODE 68911	
JET PROPULSION LABORATORY CALIFORNIA INSTITUTE OF TECHNOLOGY				
CAGE NO. 23835				
Procurement Specification: CS515577		TITLE: MICROCIRCUIT, CMOS, LINEAR ANALOG-TO-DIGITAL CONVERTER, 14-BIT		
Screening Specification: ZPP-2073-GEN				
Custodian: Electronic Parts Reliability Section 514				
		DETAIL SPECIFICATION		
		ST 12196		
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- 7/ FOR FLIGHT PARTS, THE FOLLOWING ADDITIONAL REQUIREMENTS/DETAILS SHALL APPLY:
- A. SCREENING AND QCI IN ACCORDANCE WITH TABLE V HEREIN (TBD) ARE REQUIRED.
 - B. THE MANUFACTURER SHALL MAINTAIN TRACEABILITY FROM EACH SERIALIZED DEVICE TO THE INDIVIDUAL WAFER.
 - C. THE MANUFACTURER SHALL STORE DICE IN A CLEAN, DRY ENVIRONMENT AND TAKE EXTREME CARE IN HANDLING THEM.
 - D. THE MANUFACTURER SHALL PERFORM ELEMENT EVALUATION PER MIL-STD-883, METHOD 5008.
 - E. NO DELIDDING FOR REWORK SHALL BE PERMITTED AFTER THE PACKAGE HAS BEEN SEALED.
 - F. CONTROL UNITS SHALL BE USED IN ACCORDANCE WITH CS515577 ¶3.1.3.34
 - G. JPL SOURCE INSPECTION IS REQUIRED AT PRE-SEAL, COMPLETION OF ASSEMBLY, COMPLETION OF SCREENING, AND FINAL LOT ACCEPTANCE AT COMPLETION OF QCI. THE MANUFACTURER SHALL NOTIFY JPL AT LEAST 72 HOURS IN ADVANCE OF SOURCE INSPECTION REQUIREMENTS.
 - H. THE MANUFACTURER SHALL NOTIFY THE JPL CONTRACT TECHNICAL MANAGER OF SIGNIFICANT PROBLEMS IN ACCORDANCE WITH CS515577 ¶3.10.
 - I. ALL REJECTS SHALL BE IDENTIFIED, PACKAGED SEPARATELY, AND DELIVERED TO JPL UPON COMPLETION OF TESTING.
- 8/ FOR EM PARTS, THE FOLLOWING REQUIREMENTS SHALL APPLY:
- A. ASSEMBLY SHALL BE IDENTICAL TO THE FLIGHT UNITS.
 - B. DICE USED SHALL BE FROM THE SAME MANUFACTURER AS FLIGHT UNITS.
 - C. FINISHED UNITS SHALL MEET REQUIREMENTS OF TABLE III HEREIN OVER THE OPERATING TEMPERATURE RANGE.
9. THIS STANDARD TAKES PRECEDENCE OVER DOCUMENTS REFERENCED HEREIN.

ADDITIONAL REQUIREMENTS FOR PACKAGED PARTS:

1. THE MANUFACTURER SHALL ESTABLISH BASELINE DOCUMENTATION SUFFICIENT TO COMPLETELY DEFINE AND CONTROL THE CONFIGURATION OF DEVICES SUPPLIED. THE DOCUMENTATION SHALL FORM THE BASIS FOR DEFINING THE DEVICE QUALIFIED TO THIS SPECIFICATION AND ALL DEVICES SUPPLIED ON SUBSEQUENT PROCUREMENT SHALL BE THE SAME AS THAT QUALIFIED. NO CHANGES IN CONSTRUCTION, TECHNOLOGY, OR MANUFACTURING PROCESSING SHALL OCCUR WITHOUT JPL NOTIFICATION AND APPROVAL.
2. A SAMPLE OF THE FLATPAK PACKAGED UNITS SHALL BE SUBJECTED TO AND PASS THE GROUP D PACKAGE QUALIFICATION TESTS PER MIL-STD-883, METHOD 5005, TABLE IV, EXCEPT THAT THE SUBGROUP 5 SALT ATMOSPHERE TEST IS NOT REQUIRED. THIS TEST SHALL BE PERFORMED AS SOON AS POSSIBLE AFTER ASSEMBLY IS COMPLETED.
3. JPL'S RADIATION TEST GROUP SHALL PERFORM TOTAL DOSE CHARACTERIZATION PER MIL-STD-883, METHOD 5005, GROUP E, SUBGROUP 2. THIS TEST SHALL BE PERFORMED AS SOON AS POSSIBLE AFTER ASSEMBLY IS COMPLETED.
4. THE MANUFACTURER SHALL TAKE PARTICULAR CARE TO ENSURE THAT IN-PROCESS DIE ATTACH MONITORS ARE IN EFFECT.
5. THE MANUFACTURER SHALL PERFORM, AND DELIVER TO JPL, WORST CASE AND STRESS ANALYSES.
6. THE MANUFACTURER SHALL SUBMIT FOR JPL REVIEW AND APPROVAL THE FOLLOWING:
 - A. A PROCUREMENT PLAN FOR THE FLATPACK PACKAGES WHICH SHOWS THE SCREENING, LOT TESTS, AND INTENDED QUALIFICATIONS.
 - B. DOCUMENTATION WHICH IDENTIFIES ALL OF THE PROCESSES AND CONTROLS, INSPECTIONS, AND TEST STEPS TO BE USED IN THE MANUFACTURING AND TEST OF DEVICES TO BE SUPPLIED TO THIS SPECIFICATION. THIS SHALL INCLUDE:
 - THE DIE-ATTACH AND BONDING OPERATIONS DETAILS
 - THE MANUFACTURER'S INTERNAL ESD CONTROL PROCEDURE
 - PROVISIONS FOR IN-PROCESS JPL SOURCE INSPECTION
 - C. THE ASSEMBLY, ELEMENT EVALUATION, SCREENING, AND QCI TRAVELERS TO BE USED ON-LINE TO MANUFACTURE AND TEST THE DEVICES.
 - D. THE ELECTRICAL TEST PROGRAM TO BE USED TO TEST THE DEVICES, ALONG WITH A COPY OF SAMPLE TEST DATA TAKEN ON THREE DEVICES OVER THE -40°C TO +85°C TEMPERATURE RANGE.
7. THE FOLLOWING TEST DATA SHALL BE SUPPLIED WITH SHIPMENTS OF FLIGHT PARTS:
 - A. A COPY OF THE COMPLETED LOT TRAVELER(S) USED FOR ELEMENT EVAL, ASSEMBLY, SCREENING, AND QCI.
 - B. A COPY OF ATTRIBUTES TEST DATA, INCLUDING ELEMENT EVALUATION, SCREENING, AND QCI.
 - C. ELECTRICAL TEST DATA FOR ALL SPECIFIED TESTS, INCLUDING DELTA CALCULATIONS AND CONTROL UNIT DATA
 - D. CERTIFICATES OF CONFORMANCE AS APPLICABLE

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TABLE II. ELECTRICAL TEST REQUIREMENTS

TEST	SUBGROUPS
PRE BURN-IN	1, 7
POST STATIC I (96-HOUR) BURN-IN 1/ 4/	1, 7
DELTA CALCULATIONS 2/	
POST STATIC II (96 HOUR) BURN-IN 1/ 4/	1, 7
DELTA CALCULATIONS 2/	
POST DYNAMIC (240-HOUR) BURN-IN 3/ 5/	1, 2, 3, 4, 7, 8, 9, 10, 11, 12
DELTA CALCULATIONS 2/	
GROUP B.5 500-HOUR INTERIM MEASUREMENT	1, 7
GROUP B END POINTS 3/	1, 2, 3, 4, 7, 8, 9, 10, 11, 12

NOTES FOR TABLE II:

- 1/ STATIC I, BURN-IN CIRCUIT SHALL BE PER FIGURE 2 HEREIN.
 STATIC II, BURN-IN CIRCUIT SHALL BE PER FIGURE 3 HEREIN.
 2/ DELTA LIMIT SHALL BE IN ACCORDANCE WITH TABLE IV HEREIN.
 3/ DYNAMIC BURN-IN AND LIFE TEST CIRCUIT SHALL BE PER FIGURE 4 HEREIN.
 4/ FOR ST12196-U7872FXB, BURN-IN DURATION= 24 HRS.
 5/ FOR ST12196-U7872FXB, BURN-IN DURATION=160 HRS.

TABLE III. AD7872

PARAMETER	J, A Versions ¹	K, B Versions ¹	T Version ¹	UNITS	TEST CONDITIONS/ COMMENTS
DYNAMIC PERFORMANCE²					
SIGNAL TO NOISE RATIO ³ (SNR) @ +25°C	80	80	79	DB MIN	V _{IN} = 10kHz SINE WAVE
T _{MIN} TO T _{MAX}	80	80		DB MIN	SNR IS TYPICALLY 82 DB FOR
TOTAL HARMONIC DISTORTION (THD)	-86	-90		DB MAX	<V _{IN} <41.5kHz;
				DB TYP	V _{IN} = 10kHz SINE WAVE
PEAK HARMONIC OR SPURIOUS NOISE	-86	-90		DB MAX	V _{IN} = 10kHz
				DB TYP	
INTERMODULATION DISTORTION (IMD)	-86	-90		DB MAX	FA = 9kHz, FB = 9.5kHz, F _{SAMPLE} = 50kHz
SECOND ORDER TERMS				DB TYP	
THIRD ORDER TERMS	-86	-90		DB MAX	FA = 9kHz, FB = 9.5kHz, F _{SAMPLE} = 50kHz
				DB TYP	
TRACK/HOLD ACQUISITION TIME	2	2		μS MAX	
DC ACCURACY					
RESOLUTION	14	14	14	BITS	
MINIMUM RESOLUTION FOR WHICH NO MISSING CODES ARE GUARANTEED	14	14	14	BITS	
INTEGRAL NONLINEARITY @ +25°C	±1/2	±1/2	±1/2	LSB TYP	
INTEGRAL NONLINEARITY	±1	±1	±1	LSB MAX	
BIPOLAR ZERO ERROR	±12	±12	±12	LSB MAX	
POSITIVE GAIN ERROR ⁴	±12	±12	±12	LSB MAX	
NEGATIVE GAIN ERROR ⁴	±12	±12	±12	LSB MAX	
ANALOG INPUT					
INPUT VOLTAGE RANGE	±3	±3	±3	VOLTS	
INPUT CURRENT	±500	±500	±500	μA MAX	
REFERENCE OUTPUT					
REF OUT @ +25°C	2.99/3.01	2.99/3.01	2.99/3.01	V MIN/V MAX	
T _{MIN} TO T _{MAX}	2.98/3.02	2.98/3.02	2.98/3.02	V MIN/V MAX	
REF OUT TEMPCO		±40	±40	PPM/°C MAX	TYPICALLY 35 PPM
REFERENCE LOAD SENSITIVITY (Δ REF OUT/Δ I)	±1	±1	±1	mV MAX	REFERENCE LOAD CURRENT CHANGE (0- 500μA); REFERENCE LOAD SHOULD NOT BE CHANGED DURING CONVERSION
LOGIC INPUTS					
INPUT HIGH VOLTAGE V _{INH}	2.4	2.4	2.4	V MIN	V _{DD} = 5V ± 5%
INPUT LOW VOLTAGE V _{INI}	0.8	0.8	0.8	V MAX	V _{DD} = 5V ± 5%
INPUT CURRENT, I _{IN}	±10	±10	±10	μA MAX	V _{IN} = 0V TO V _{DD}
INPUT CURRENT (14/9/CLK INPUT ONLY)	±10	±10	±10	μA MAX	V _{IN} = V _{SS} TO V _{DD}
INPUT CAPACITANCE, C _{IN} ⁵	10	10	10	pF MAX	
LOGIC OUTPUTS					
OUTPUT HIGH VOLTAGE, V _{OH}	4.0	4.0	4.0	V MIN	I _{SOURCE} = 40 μA
OUTPUT LOW VOLTAGE, V _{OL}	0.4	0.4	0.4	V MAX	I _{SINK} = 1.6 mA

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TITLE:

MICROCIRCUIT, CMOS, LINEAR
 ANALOG-TO-DIGITAL CONVERTER, 14-BIT

ST 12196

REV. B

SHEET OF

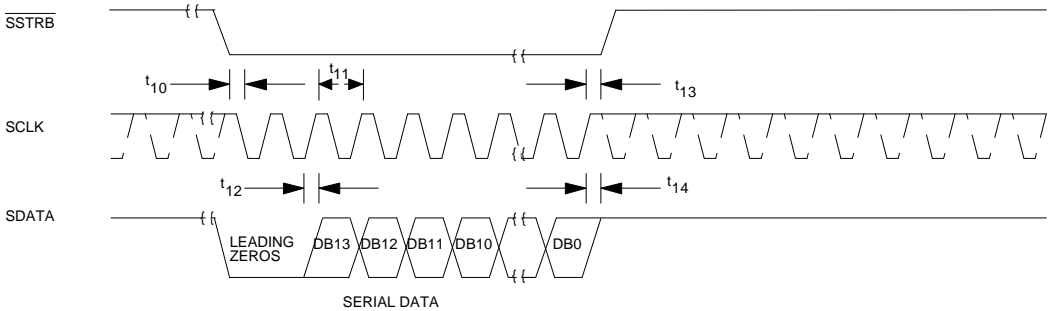
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CONVERSION TIME EXTERNAL CLOCK INTERNAL CLOCK	10 10.5	10 10.5	10 10.5	μ S MAX μ S MAX	THE INTERNAL CLOCK HAS A NOMINAL VALUE OF 2 MHz
POWER REQUIREMENTS V_{DD} V_{SS} I_{DD} I_{SS} POWER DISSIPATION	+5 -5 13 6 95	+5 -5 13 6 95	+5 -5 13 6 95	V NOM V NOM mA MAX mA MAX mW MAX	\pm 5% FOR SPECIFIED PERFORMANCE \pm 5% FOR SPECIFIED PERFORMANCE TYPICALLY 6 mA TYPICALLY 4 mA TYPICALLY 50 mW

- NOTES
- ¹TEMPERATURE RANGES ARE AS FOLLOWS: J, K VERSIONS, 0°C TO +70°C; A, B VERSIONS, -40°C TO +85°C; T VERSION; -55°C TO +125°C.
- ² $V_{IN} = \pm 3V$. NOT TESTED BUT GUARANTEED BY DESIGN.
- ³SNR CALCULATION INCLUDES DISTORTION AND NOISE COMPONENTS.
- ⁴MEASURED WITH RESPECT TO INTERNAL REFERENCE.

Table III. CONT'D

PARAMETER	LIMIT AT T _{min} , T _{max} (J, K, A, B Versions)	LIMIT AT T _{min} , T _{max} (T Version)	UNITS	CONDITIONS/COMMENTS
T ₁	50	50	NS MIN	CONVST PULSE WIDTH
T _{10₂}	100	100	NS MIN	SSTRB TO SCLK FALLING EDGE SETUP TIME
T _{11₁}	440	440	NS MIN	SCLK CYCLE TIME
T ₁₂	155	155	NS MAX	SCLK TO VALID DATA DELAY. C _I = 35 pF
T ₁₃	140	150	NS MAX	SCLK RISING EDGE TO SSTRB
	20	20	NS MIN	
T ₁₄	4	4	NS MIN	BUS RELINQUISH TIME AFTER SCLK
	100	100	NS MAX	



MODE 1 TIMING DIAGRAM, BYTE OR SERIAL READ

- NOTES
- ¹ ALL INPUT SIGNALS ARE SPECIFIED WITH $t_r = t_f = 5$ ns (10% TO 90% OF 5 V) AND TIMED FROM A VOLTAGE LEVEL OF 1.6 V.
- ²SERIAL TIMING IS MEASURED WITH A 4.7K Ω PULL-UP RESISTOR ON SDATA AND SSTRB AND A 2K Ω PULL-UP RESISTOR ON SCLK. THE CAPACITANCE ON ALL THREE OUTPUTS IS 35 pF.
- ³SCLK MARK/SPACE RATIO (MEASURED FROM A VOLTAGE LEVEL OF 1.6 V) IS 40/60 TO 60/40.
- ⁴SDATA WILL DRIVE HIGHER CAPACITIVE LOADS, BUT THIS WILL ADD TO T₁₂ SINCE IT INCREASES THE EXTERNAL RC TIME CONSTANT (4.7 K Ω /C_L) AND HENCE THE TIME TO REACH 2.4 V.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} TO AGND..... -0.3 V TO +7 V
 V_{SS} TO AGND..... +0.3 V TO -7 V
AGND TO DGND..... -0.3 V TO $V_{DD} + 0.3$ V
 V_{IN} TO AGND..... $V_{SS} - 0.3$ V TO $V_{DD} + 0.3$ V
REF OUT, C_{REF} TO AGND..... 0 V TO V_{DD}
DIGITAL INPUTS TO DGND..... -0.3 V TO $V_{DD} + 0.3$ V
DIGITAL OUTPUTS TO DGND..... -0.3 V TO $V_{DD} + 0.3$ V
OPERATING TEMPERATURE RANGE
COMMERCIAL (J, K VERSIONS)..... 0°C TO +70°C
INDUSTRIAL (A, B VERSIONS)..... -40°C TO +85°C

EXTENDED (T VERSION)..... -55°C TO +125°C
STORAGE TEMPERATURE RANGE..... -65°C TO +150°C
LEAD TEMPERATURE (SOLDERING, 10 SECS)..... +300°C
POWER DISSIPATION (ANY PACKAGE) TO +75°C. 450 mW
DERATES ABOVE +75°C BY..... 6 mW/°C

* STRESSES ABOVE THOSE LISTED UNDER "ABSOLUTE MAXIMUM RATINGS" MAY CAUSE PERMANENT DAMAGE TO THE DEVICE. THIS IS A STRESS RATING ONLY AND FUNCTIONAL OPERATION OF THE DEVICE AT THESE OR ANY OTHER CONDITIONS ABOVE THOSE LISTED IN THE OPERATIONAL SECTIONS OF THIS SPECIFICATION IS NOT IMPLIED. EXPOSURE TO ABSOLUTE MAXIMUM RATING CONDITIONS FOR EXTENDED PERIODS MAY AFFECT DEVICE RELIABILITY.

TABLE III. DELTA LIMITS

PARAMETER	SYMBOLS	PARAMETER LIMITS		UNITS	DELTA LIMITS
		MIN	MAX		
SUPPLY CURRENT	I _{DD}	-	+13	mA	\pm 10%
SUPPLY CURRENT	I _{SS}	-6	-	mA	\pm 10%

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INPUT CURRENT	I _{IN}	-1Ø	+1Ø	µA	±200% µA
OUTPUT LOW CURRENT @ .4V	I _{OL}	1.6		mA	±15%

TABLE IV. SUMMARY OF ASSEMBLY & TEST OF PACKAGED PARTS

	OPERATION	883 METHOD
Assembly	Element evaluation (using Rad-Pak packaging)	5ØØ8, Table III
	JPL review of documentation (travelers, test programs, etc.)	
	Assembly - including: JPL precap inspection 1ØØ% non-destructive bond pull	2Ø1Ø, Cond.A 2Ø23
	Post-assembly JPL visual inspection	
	Go/No go electricals at 3 temps.	
	(Ship EM parts)	
Early QCI	Group D except delete salt atmosphere test of subgroup 5	5ØØ5, Table IV
	Group E subgroup 2 total dose radiation test to 1ØØ krad	5ØØ5, Table V
Screening	Temperature cycling	1Ø1Ø, Cond.C
	Constant acceleration	2ØØ1, Cond.E (min), Y ₁ only
	Visual inspection	
	PIND	2Ø2Ø, Cond.A
	Serialization (may be done at any time prior to this)	
	Burn-ins & electrical tests, & delta calculations per ST12Ø75 Tables II & III	
	PDA calculation	5ØØ4
	Fine & gross leak	1Ø14
	External visual (w/JPL source insp.)	2ØØ9
	JPL selection of QCI samples	
	(Note: JPL may direct shipment of screened parts at this point.)	
QCI	Group B, Subgroups 1-4	5ØØ5, Table IIa
	Group B, Subgroup 5, but including interim R/R of subgroups 1&7 at 5ØØ hours	5ØØ5, Table IIa
	Fine & gross leak of life test parts	1Ø14
	Final shipment (w/JPL source inspection)	

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Filename: ST12196B.DOC
Directory: H:\USERS\514\SPECS\ACT-DETL
Template: F:\USERS\MARITZA\WINWORD\SPEC.DOT
Title:
Subject:
Author: Maritza R Davis
Keywords:
Comments:
Creation Date: 09/26/94 10:12 AM
Revision Number: 11
Last Saved On: 09/27/94 8:38 AM
Last Saved By: Maritza R Davis
Total Editing Time: 66 Minutes
Last Printed On: 08/08/95 9:56 AM
As of Last Complete Printing
Number of Pages: 5
Number of Words: 2,260 (approx.)
Number of Characters: 12,884 (approx.)